PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of

Jae-jun MOON, et al.

Appln. No.: 10/777,097

Confirmation No.: 4555

Filed: February 13, 2004

For: BIAS CIRCUIT HAVING START-UP CIRCUIT

Docket No: Q77183

Group Art Unit: 2816

Examiner: Jeffery Shawn Zweizig

SUBMISSION OF APPEAL BRIEF

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith please find an Appeal Brief. A check for the statutory fee of $500.00 is attached. The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account. A duplicate copy of this paper is attached.

Respectfully submitted,

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Date: February 28, 2006

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APPEAL BRIEF UNDER 37 C.F.R. § 41.37

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Sir:

In accordance with the provisions of 37 C.F.R. § 41.37, Appellant hereby submits this Appeal Brief, appealing the final Office Action dated August 30, 2005 (hereinafter "the final Office Action), finally rejecting claims 1-4. This Appeal Brief is accompanied by a Submission including the required appeal fee set forth in 37 C.F.R. § 41.20(b)(2) and a Petition for Extension of Time. Appellant's Notice of Appeal was filed on November 30, 2005. Therefore, the present Appeal Brief is timely filed.

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I. REAL PARTY IN INTEREST

The real party in interest is SAMSUNG ELECTRONICS CO., LTD., (Assignee) by virtue of an assignment executed by the inventors (Appellant), Jae-jun MOON, Jeong-won LEE, and Jung-eun LEE, on February 5, 2004, and recorded by the Assignment Branch of the U.S. Patent and Trademark Office on February 13, 2004 (at Reel 014989, Frame 0832).

II. RELATED APPEALS AND INTERFERENCES

Upon information and belief, there are no other prior or pending appeals, interferences, or judicial proceedings known to Appellant, Appellant's representatives or the Assignee that may be related to, be directly affected by, or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claims 1-4 are all the claims pending in the application.

Claims 1 and 3 are rejected under 35 U.S.C. § 102(b) as being anticipated by Wu et al. (U.S. Patent No. 5,307,007).

Claims 1-4 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki (U.S. Patent No. 5,180,967) in view of Wu et al.

Claims 1-4, which have been at least twice rejected, are the claims on appeal (See Claims Appendix).

IV. STATUS OF AMENDMENTS

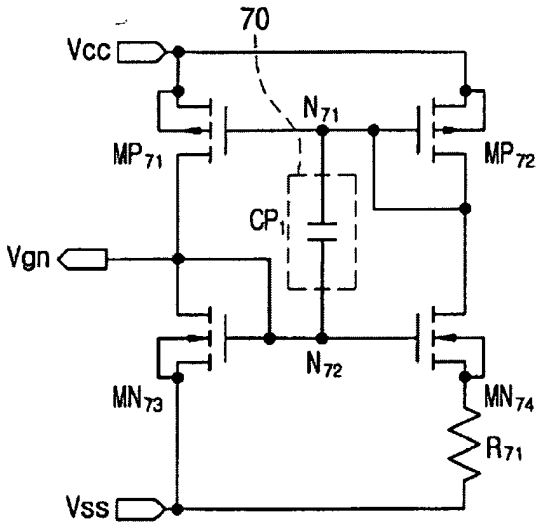
The claims on appeal, claims 1-4, have not been amended subsequent to the final rejection of August 30, 2005.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

The present invention relates to a bias circuit having a start-up circuit. See Abstract of Appellant's Specification. The start-up circuit prevents noise caused by power source voltage and power consumption due to static currents and provides improved stability at high frequencies. See id.

An embodiment of the bias circuit shown in Fig. 7 is reproduced below:

FIG. 7



Claims 1 and 2

An embodiment of the present invention provides a bias circuit having a bias circuit part and a start-up circuit. The bias circuit part uses a current mirror circuit and generates a constant bias voltage at an output node from a power source as applied.

The embodiment further includes a start-up circuit having a capacitor connected between the output node and a common node of in common connecting gates of MOS transistors constructing the current mirror circuit.

Claims 3 and 4

Another embodiment of the invention includes a bias circuit having a bias circuit part and a start-up circuit part. The bias circuit part uses a cascode current mirror circuit of a double-stage current mirror circuit and generates a constant bias voltage to an output node from an applied power source voltage.

The start-up circuit part actuates the bias circuit part upon an initial application of the power source voltage. The start-up circuit part includes a first capacitor and a second capacitor.

The first capacitor is connected between a first common node and a second common node. The first common node connects in common gates of first MOS transistors constructing a first single-stage current mirror circuit of the cascode current mirror circuit. The second common node connects in common gates of second MOS transistors constructing a second single-stage current mirror circuit.

There is also a second capacitor connected between the second common node and the output node.

Means-Plus-Function Claims

No means-plus-function or step-plus-function has been identified among the claims on appeal.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 1 and 3 are rejected under 35 U.S.C. § 102(b) as being anticipated by Wu et al. (U.S. Patent No. 5,307,007; hereinafter "Wu").

2. Claims 1-4 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki (U.S. Patent No. 5,180,967; hereinafter "Yamazaki") in view of Wu.

VII. ARGUMENT

Applicant respectfully submits that claim 1 is believed to be patentable because Wu fails to disclose each and every element of the claim. Claim 1 recites:

> A bias circuit having a start-up circuit, comprising:
>
> a bias circuit part using a current mirror circuit, and for generating a constant bias voltage to an output node from a power source voltage as applied, and
>
> a start-up circuit part having a capacitor connected between the output node and a common node of in common connecting gates of MOS transistors constructing the current mirror circuit.

(Emphasis added).

For example, Wu fails to disclose or suggest, inter alia, a bias circuit part using a current mirror circuit, and for generating a constant bias voltage to an output node from a power source voltage as applied, and a start-up circuit part having a capacitor connected between the output node and a common node the bias circuit and the start-up circuit, as recited in the claim.

In the Final Office Action, the Examiner states that the node between the NMOS transistors M1 and M3 corresponds to the claimed output node. See paragraph 2 at page 2. In the Response to Arguments section of the Final Office Action, the Examiner states that the output from the gate of the NMOS transistor M3 in Fig. 1 is an output of the circuit formed by the NMOS transistors M3-M8, resistor R1, and capacitors C1 and C2. According to the Examiner, this output allegedly corresponds to the claimed output node. Applicant respectfully disagrees.

First, this particular node at the gate of NMOS transistor M3 cannot correspond to the claimed output node. This particular node is merely connected to the gate of PMOS transistor M1, the gate of the NMOS transistor M3, the gate of the NMOS transistor M4, the capacitor C_1 and the source/drains of the NMOS transistor M3 and M4. Therefore, there is no way for this particular node to provide any sort of output, and thus, cannot possibly correspond to the claimed output node.

Applicant points out that in a description of an embodiment of the invention, "an output voltage Vgn is outputted through the output node." Paragraph 43 of Specification and Fig. 7. In contrast, there is absolutely nothing at the gate of the NMOS transistor M3 which would allow the output or the detection of any voltage at the gate.

Second, the Examiner's argument that the gate of M3 corresponds to the claimed output node ignores the distinctions made in claim 1 between the recited common node and output node. In claim 1, the start-up circuit part is recited as having a common node of in common connecting gates of MOS transistors and separately recites an output node to which a constant bias voltage is generated. With this recitation of two different types of nodes, the gate of M3 cannot be characterized as corresponding to the claimed output node given the separate recitation of a common node in the claim.

Not only does Wu fail to expressly disclose an output node, Wu also fails to inherently disclose an output node.

"To establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would

be so recognized by persons of ordinary skill." M.P.E.P. § 2112(IV) (quoting In re Robertson, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999)). Moreover, "[t]he fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic." Id. (quoting In re Rijckaert, 9 F.3d 1531, 1534 (Fed. Cir. 1993) (reversed rejection because inherency was based on what would result due to optimization of conditions, not what was necessarily present in the prior art)).

In the Office Action, a basis or a technical reasoning for having the claimed output node in Wu is not provided. For example, there is no rationale for outputting a voltage at the node between the NMOS transistors M1 and M3 to reasonably support the determination that the output node of claim 1 is necessarily present in Wu.

Admittedly, Wu does disclose outputting a voltage level, i.e., V_{out}, but this voltage is outputted at an entirely different location at the transistor Q_3 as shown in Fig. 1. Here, the mere fact that there may be an output node at the gate of NMOS transistor M4, when such a node is clearly not disclosed, is not sufficient to support the supposed inherent disclosure of the claimed output node in Wu. Since Wu fails to disclose or suggest all claim elements, claim 1 is not anticipated by Wu and thus, believed to be patentable.

Similarly, Wu fails to disclose or suggest an output node wherein a second capacitor is connected between the second common node and the output node, as recited in claim 3. The Examiner characterizes a node between M4 and M6 as corresponding to the claimed output node. This node, however, is merely connected to the capacitor C1, the gates of M3 and M4, the

source/drain of M4, and the source/drain of M6, and not to any sort of output. For at least the above reasons, claim 3 is not anticipated by Wu and believed to be patentable.

Rejections of Claims 1-4 under § 103(a) over Yamazaki in view of Wu

Applicant respectfully submits that claim 1 is believed to be patentable because Yamazaki in view of Wu fail to teach, suggest or provide motivation for, inter alia, the claimed output node as recited in the claim. There is nothing in the references which supports the conclusion that the claimed output node is necessarily present in the combination of Yamazaki and Wu. Therefore, Yamazaki in view of Wu cannot inherently disclose such an output node. Therefore, claims 1 and 3 are believed to be patentable.

In addition, Yamazaki and Wu do not expressly disclose the claimed output node. Although the Examiner mentions nodes N11 or N12 of Yamazaki, there is nothing in Yamazaki that suggests that these nodes correspond to the claimed output node. Instead, the node N11 is connected to the drain and the gate of the PMOS 104, the gate of the PMOS 106, the gate of the PMOS transistor 116, the drain of the NMOS transistor 118, and the drain of the NMOS transistor 112. Node N12 is connected to the drain of the PMOS transistor 105, the drain of the PMOS transistor 120, and the gate and the drain of the NMOS transistor 110. Yamazaki fails to disclose the claimed output node and, thus, claim 1 is believed to be patentable.

Claim 3 is believed to be patentable because the node between the PMOS transistor 126 and the NMOS transistor 128 are not connected to any sort of an output node. Thus, claim 3 is believed to be patentable.

Claim 2, which depends from claim 1, and claim 4, which depends from claim 3 are patentable for at least the reasons submitted for their respective base claims.

In addition, claim 4 is patentable because Yamazaki in view of Wu fail to teach, suggest or provide motivation for all elements of the claim. Claim 4 recites, inter alia:

> 4. (original): The bias circuit as claimed in claim 3, wherein the bias circuit part includes:
>
> . . . ;
>
> a fourth PMOS transistor having a gate and a drain thereof connected to a gate of the first PMOS transistor to form a second common node, and having a source thereof connected to the drain of the second PMOS transistor;
>
> a first NMOS transistor having a drain and a gate thereof connected to a drain of the third PMOS transistor to form the output node, and having a source thereof connected to a grounded power source;
>
> . . . .

For example, Yamazaki in view of Wu fail to teach, suggest or provide motivation for a fourth PMOS transistor having a gate and a drain thereof connected to a gate of the first PMOS transistor to form a second common node, and a first NMOS transistor having a drain and a gate thereof connected to a drain of the third PMOS transistor to form the output node, in combination with other elements of the claim.

In the Final Office Action, the Examiner argues that PMOS 106 and PMOS 124 of Fig. 5 in Yamazaki correspond to the claimed first PMOS and the fourth PMOS. See page 3. Assuming arguendo, that the Examiner is correct, the PMOS 124 does not have a gate and a drain thereof connected to a gate of the PMOS 106. Rather, the gate and the drain of the PMOS 124 are connected to the gate of the PMOS 126 which the Examiner characterizes as corresponding to the claimed third PMOS transistor.

VIII. CONCLUSION

In view of the foregoing, Appellant submits that the Examiner has failed to show how claims 1 and 3 are anticipated and to establish a prima facie case of obviousness with respect to claims 1-4. Therefore, the rejection of claims 1-4 under 35 U.S.C. § 102(b) and 103(a) is improper and should be reversed.

Unless a check is submitted herewith for the fee required under 37 C.F.R. §41.37(a) and 1.17(c), please charge said fee to Deposit Account No. 19-4880.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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CLAIMS APPENDIX

CLAIMS 1-4 ON APPEAL:

1. A bias circuit having a start-up circuit, comprising:

a bias circuit part using a current mirror circuit, and for generating a constant bias voltage to an output node from a power source voltage as applied, and

a start-up circuit part having a capacitor connected between the output node and a common node of in common connecting gates of MOS transistors constructing the current mirror circuit.

2. The bias circuit as claimed in claim 1, wherein the bias circuit part includes:

a first PMOS transistor having a source thereof connected to the power source voltage;

a second PMOS transistor having a gate and a drain thereof connected to a gate of the first PMOS transistor to form the common node, and having a source thereof connected to the power source voltage;

a first NMOS transistor having a drain and a gate thereof connected to a drain of the first PMOS transistor to form the output node, and having a source thereof connected to a grounded power source;

a second NMOS transistor having a drain thereof connected to the drain of the second PMOS transistor, and having a gate thereof connected to the gate of the first NMOS transistor; and

a resistor connected between the source of the second NMOS transistor and the grounded power source.

3. A bias circuit having a start-up circuit, comprising:

a bias circuit part using a cascode current mirror circuit of a double-stage current mirror circuit, and for generating a constant bias voltage to an output node from an applied power source voltage; and

a start-up circuit part for actuating the bias circuit part upon an initial application of the power source voltage, the start-up circuit part including:

a first capacitor connected between a first common node connecting in common gates of first MOS transistors constructing a first single-stage current mirror circuit of the cascode current mirror circuit and a second common node connecting in common gates of second MOS transistors constructing a second single-stage current mirror circuit; and

a second capacitor connected between the second common node and the output node.

4. The bias circuit as claimed in claim 3, wherein the bias circuit part includes:

a first PMOS transistor having a source thereof connected to the power source voltage;

a second PMOS transistor having a gate and a drain thereof connected to a gate of the first PMOS transistor to form the first common node, and having a source thereof connected to the power source voltage;

a third PMOS transistor having a source thereof connected to a drain of the first PMOS transistor;

a fourth PMOS transistor having a gate and a drain thereof connected to a gate of the first PMOS transistor to form a second common node, and having a source thereof connected to the drain of the second PMOS transistor;

a first NMOS transistor having a drain and a gate thereof connected to a drain of the third PMOS transistor to form the output node, and having a source thereof connected to a grounded power source;

a second NMOS transistor having a drain thereof connected to the drain of the fourth PMOS transistor, and having a gate thereof connected to the gate of the first NMOS transistor; and

a resistor connected between a source of the second NMOS transistor and the grounded power source.

EVIDENCE APPENDIX:

This Appendix is not applicable to this Appeal.

RELATED PROCEEDINGS APPENDIX

This Appendix is not applicable to this Appeal.